--12. (New) In a dot matrix display having a plurality of scan lines and a plurality of signal lines arranged in matrix form, a display element coupled between each scan line and signal line at an intersecting point, a circuit to reduce erroneous activation of the display element comprising:

a reduced voltage source having an output voltage less than a voltage used to drive the display element;

a discharge circuit for coupling each of the scan lines to the voltage source at a time when the scan line is not activating a display element, whereby charge accumulating at a display element is discharged to reduce erroneous activation of the display element.

13. (New) The display of Claim 12 wherein the dot matrix display is a light emitting diode (LED) display.

14. (New) The display of Claim 13 wherein the discharge circuit comprises a plurality of LEDs, one LED being coupled between each scan line and the reduced voltage source for discharging charge accumulating on each of the LEDs and on the scan line.

15. (New) The display of Claim 14 wherein the discharge circuit further comprises a switch coupled between one electrode of each of the LEDs and the reduced voltage source.

16. (New) The display of Claim 15 wherein the discharge circuit comprises LEDs of one column of the matrix, the LEDs of the one column being covered so as not to form a visible part of the display.

17. (New) The display of Claim 14 wherein the discharge circuit comprises a plurality of switches, one switch being coupled between each LED and the reduced voltage source.

18. (New) The display of Claim 14 wherein the discharge circuit further comprises a current source coupled between each switch and the reduced voltage source.

19. (New) The display of Claim 17 wherein the discharge circuit further comprises a current source coupled between each switch and the reduced voltage source.

20. (New) The display of Claim 12 wherein the discharge circuit comprises a plurality of resistors, each resistor being coupled between one scan line and the reduced voltage source.

21. (New) The display of Claim 12 wherein the discharge circuit further comprises a plurality of scan line buffer circuits each coupling a scan line to the reduced voltage source when not driving a display element.

22. (New) The display of Claim 21 wherein each buffer circuit couples its respective scan line to a driving voltage source when it is driving the display element.

23. (New) The display of Claim 12 wherein the reduced voltage source is at the reference potential.

24. (New) The display of Claim 15 wherein the reduced voltage source is at the reference potential.

25. (New) The display of Claim 17 wherein the reduced voltage source is at the reference potential.

26. (New) The display of Claim 18 wherein the reduced voltage source is at the reference potential.